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| JOHNSON, BRIAN P | |

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DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/743,711 | JOURDAN ET AL. | |
| | Examiner | Art Unit | |
| | Brian P. Johnson | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-24,26,27 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-24, 26, 27, 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1, 3-24, 26-27, 29-34 are pending.

### *Papers Filed*

2. Examiner acknowledges receipt of amendments and remarks filed on 19 July 2006.

### *Title*

3. The title is accepted. Objection is withdrawn.

### *Claim Objections*

***1.*** In light of Applicant's amendment, objection is withdrawn.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 5-6, 16-19, 21-24, 27, 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biles in view of Yeh et al. (U.S. Publication No. 2001/0047467) hereinafter referred to as Yeh.

6. As per claim 1, Biles teaches a branch prediction architecture comprising:

a prediction selector; (Fig. 2b parts 230, 220, 225, 240, 260, 250)

a bimodal predictor (Fig. 2b table 210) coupled to the prediction selector, the bimodal predictor to generate a bimodal prediction for a branch instruction; (Paragraph 59)

and a plurality of global predictors (Fig. 2b tables 205, 207) coupled to the prediction selector, each global predictor to generate a corresponding global prediction for the branch instruction, (paragraphs 58 and 60) the prediction selector to select a branch prediction from the bimodal prediction and the global predictions. (Paragraph 67) Biles but fails to teach wherein each global prediction is to be generated based on a different amount of global branch history information.

Yeh teaches two global predictions (Fig. 2 tables 21 and 22) generated based on a different amount of global branch history information. *The examiner asserts that Yeh's invention discloses branch prediction tables of varied sizes (paragraph 10).*

7. Yeh teaches that tables of various sizes "provide a solution that yields low latency branch predictions for the most frequent subset of branches and yet provides meaningful predictions for the overall working set" (paragraph 8).

8. It would have been obvious to one of ordinary skill in the art at the time of invention to have used Yeh's scheme of using differently sized tables in place of Biles' tables 205 and 207 to store branch predictions for the benefit of providing both low latency accesses when possible and a large working set when the low latency access are not possible.

9. The examiner notes that a larger table inherently requires a value with a number of bits to index. The combination of Biles and Yeh would inherently use more global history to index into the larger of the global history tables than the smaller table would require.

10. As per claim 3, Biles and Yeh teach the branch prediction architecture of claim 1, wherein the plurality of global predictors includes:

a first global predictor to generate a first global prediction by indexing into a first global array based on a first index, the first index to be associated with a first amount of global branch history information; (Biles paragraph 63)

and a second global predictor to generate a second global prediction by indexing into a second global array based on a second index, the second index to be associated with a second amount of global branch history information, the first amount to be less than the second amount. *The examiner notes that a larger table inherently requires a*

*value with a number of bits to index. The combination of Biles and Yeh would inherently use more global history to index into the larger of the global history tables than the smaller table would require.*

11. As per claim 5, Biles and Yeh teach the branch prediction architecture of claim 3, wherein the branch prediction architecture is to generate the first index by shifting a most recent branch bit into a previous first global branch history to obtain a current first global branch history and performing an exclusive OR operation between the current first global branch history and one or more portions of an instruction address associated with the branch instruction, and to generate the second index by shifting the most recent branch bit into a previous second global branch history to obtain a current second global branch history and performing an exclusive OR operation between the current second global branch history and one or more portions of the instruction address, the previous and current first global branch histories to have a length that corresponds to the first amount and the previous and current second global branch histories to have a length that corresponds to the second amount. (Biles Fig. 2b and paragraph 63)

12. As per claim 6, Biles and Yeh teach the branch prediction architecture of claim 3, but fail to disclose wherein the plurality of global predictors includes a third global predictor to generate a third global prediction by indexing into a third global array based on a third index, the third index to be associated with a third amount of global branch history length, the second amount being less than the third amount.

13. Official notice is taken that adding an additional level of storage for global branch predictors is well known in the art. As disclosed by Yeh, adding an additional level of predictors provides the benefit of being able to store a larger number of entries in the additional table, while the original table(s) provide faster lookups for a smaller set of data.

14. It would have been obvious to one of ordinary skill in the art at the time of invention to add an additional table to Biles/Yeh's branch predictor for the benefit of being able to store a larger set of branch predictors while providing fast access to those more often used.

As per claim 16, Biles teaches the branch prediction architecture of claim 1, wherein the branch prediction is to include a predicted direction of the branch instruction. (paragraph 5)

15. As per claim 17, Biles/Yeh teaches the branch prediction architecture of claim 16, but fails to disclose wherein the branch prediction is to further include an instruction target address of the branch instruction.

16. Official Notice is taken that storing branch target addresses in a branch prediction table is well known in the art. Storing the address and branch direction indication in one table provides the benefit of only having to do one lookup to obtain both pieces of data in lieu of looking both up separately.

17. It would have been obvious to one of ordinary skill in the art at the time of invention to have included branch target addresses in the branch prediction tables along with the

branch direction counters for the benefit of not having to separately look up branch targets elsewhere.

18. As per claim 18, Biles and Yeh teach a branch prediction architecture comprising:

a prediction selector having a first multiplexer and a second multiplexer; (Biles Fig. 2b parts 230, 220, 225, 240, 260, 250)

a bimodal predictor coupled to the prediction selector, the bimodal predictor to generate a bimodal prediction for a branch instruction; (Biles Fig. 2b table 210)

a plurality of global predictors coupled to the prediction selector, each global predictor to generate a corresponding global prediction for the branch prediction, (Biles fig. 2b tables 205 and 207)

allocation logic coupled to the prediction selector, the allocation logic to allocate an entry in the first global array to the branch instruction if the branch prediction results in a misprediction and originated from the bimodal predictor (Fig. 8 block 570)

and update logic coupled to the predictors, the update logic to update a bimodal array of the bimodal predictor based on an actual branch outcome associated with the branch prediction, (Fig. 8 block 580)

19. Biles fails to disclose:

each global prediction to be generated based on a different amount of global branch history information.

the first multiplexer to generate an intermediate prediction based on the bimodal prediction, a first global prediction and whether a hit has occurred in a first global array,

the second multiplexer to select a branch prediction based on the intermediate prediction, a second global prediction and whether a hit has occurred in a second global array;

the allocation logic to allocate an entry in the second global array to the branch instruction if the branch prediction results in a misprediction and originated from the first global prediction;

20. Yeh discloses each global prediction to be generated based on a different amount of global branch history information. *The examiner asserts that Yeh's invention discloses branch prediction tables of varied sizes (paragraph 10).*

21. Yeh teaches that tables of various sizes "provide a solution that yields low latency branch predictions for the most frequent subset of branches and yet provides meaningful predictions for the overall working set" (paragraph 8).

22. It would have been obvious to one of ordinary skill in the art at the time of invention to have used Yeh's scheme of using differently sized tables in place of Biles' tables 205 and 207 to store branch predictions for the benefit of providing both low latency accesses when possible and a large working set when the low latency access are not possible.

23. The examiner notes that a larger table inherently requires a value with a number of bits to index. The combination of Biles and Yeh would inherently use more global history to index into the larger of the global history tables than the smaller table would require.

24. Official Notice is taken that changing the order of multiplexers is well known in the art. When three signals are to be multiplexed together, it is the designer's choice whether to switch between A and B in the first stage or to switch between B and C (or A and C) before the second stage switching between the intermediate result and the third input.

25. It would have been obvious to one of ordinary skill in the art at the time of invention to have changed Bile's multiplexing scheme to switch between the bimodal and first global table before switching between that result and the second global table. The changed system produces the same results as the first and the implementation is the choice of the system designer.

26. The examiner asserts that the combination of Biles and Yeh would inherently allocate an entry in the second global array to a branch instruction if the branch prediction results in a misprediction and originated from the first global prediction. The purpose of the larger table, requiring more branch history to index, is to provide a second storage for branch predictors which cannot be held in the first global table.

27. Claim 19 is directed toward the same limitations as claim 3, therefore it is rejected under the same grounds as recited above.

28. Claim 21 is directed toward the same limitations as claim 5, therefore it is rejected under the same grounds as recited above.

29. Claim 22 is directed toward the same limitations as claim 16, therefore it is rejected under the same grounds as recited above.

30. Claim 23 is directed toward the same limitations as claim 17, therefore it is rejected under the same grounds as recited for claim 17.

31. Claim 24 is directed toward the same limitations as claim 1, therefore it is rejected under the same grounds as recited above.

32. Claim 27 is directed toward the same limitations as claim 1, therefore it is rejected under the same grounds as recited above.

33. Claim 29 is directed toward the same limitations as claim 3, therefore it is rejected under the same grounds as recited above.

34. Claim 31 is directed toward the same limitations as claim 5, therefore it is rejected under the same grounds as recited above.

35. Claims 4, 20 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biles and Yeh in view of McFarling (U.S. Patent No. 6,374,349).

36. As per claim 4, Biles and Yeh teach the branch prediction architecture of claim 3, but fail to disclose wherein the branch prediction architecture is to generate the first index by shifting a most recent branch bit into a previous first stew to obtain a current first stew and performing an exclusive OR operation between the current first stew and one or more portions of an instruction address associated with the branch instruction, and to generate the second index by shifting the most recent branch bit into a previous second stew to obtain a current second stew and performing an exclusive OR operation between the current second stew and one or more portions of the instruction address, the previous and current first stews to have a length that corresponds to the first amount and the previous and current second stews to have a length that corresponds to the second amount.

37. McFarling teaches using a previous stew exclusive OR'd with a portion of the instruction address to generate a current stew to index into a prediction table (Fig. 12).

38. McFarling teaches that using stew code "incorporates path information into the global history register" and that the extra information may "distinguish program states that affect branch direction." (Col 10 lines 24-45) By distinguishing program states, the processor is more likely to correctly predict a branch instruction.

39. It would have been obvious to one of ordinary skill in the art at the time of invention to have included McFarling's method of generating indexes for the branch prediction tables in Biles/Yeh's processor for the benefit of distinguishing program states, thus increasing branch prediction accuracy.

40. Claim 20 is directed toward the same limitations as claim 4, therefore it is rejected under the same grounds as recited above.

41. Claim 30 is directed toward the same limitations as claim 4, therefore it is rejected under the same grounds as recited above.

42. Claims 7-15, 26 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biles/Yeh (with use of Official Notice).

43. As per claim 7, Biles/Yeh teaches the branch prediction architecture of claim 1, but fails to disclose wherein the prediction selector includes: a first multiplexer to generate an intermediate prediction based on the bimodal prediction, a first global prediction and whether a hit has occurred in a first global array; and a second multiplexer to select the branch prediction based on the intermediate prediction, a second global prediction and whether a hit has occurred in a second global array.

44. Official Notice is taken that changing the order of multiplexers is well known in the art. When three signals are to be multiplexed together, it is the designer's choice whether to switch between A and B in the first stage or to switch between B and C (or A and C) before the second stage switching between the intermediate result and the third input.

45. It would have been obvious to one of ordinary skill in the art at the time of invention to have changed Bile's multiplexing scheme to switch between the bimodal and first

global table before switching between that result and the second global table. The changed system produces the same results as the first and the implementation is the choice of the system designer.

46. As per claim 8, Biles/Yeh teaches the branch prediction architecture of claim 7, wherein the second multiplexer is to select the second global prediction if a hit notification is received from the second global array and select the intermediate prediction if a hit notification is not received from the second global array. (Fig. 2b and paragraph 81)

47. As per claim 9, Biles/Yeh teaches the branch prediction architecture of claim 8, wherein the first multiplexer is to select the first global prediction if a hit notification is received from the first global array and select the bimodal prediction if a hit notification is not received from the first global array. (Fig. 2b and paragraph 81)

48. As per claim 10, Biles/Yeh teaches the branch prediction architecture of claim 7, further including allocation logic coupled to the prediction selector, the allocation logic to allocate an entry in the first global array to the branch instruction if the branch prediction results in a misprediction and originates from the bimodal predictor. (Fig. 8 block 570)

49. As per claim 11, Biles/Yeh teaches the branch prediction architecture of claim 10, wherein the allocation logic is to allocate an entry in the second global array to the

branch instruction if the branch prediction results in a misprediction originated from a first global predictor, where the first global predictor generates the first global prediction. (Fig. 8 block 570)

50. As per claim 12, Biles/Yeh teaches the branch prediction architecture of claim 7, further including update logic coupled to the predictors, the update logic to update a bimodal array of the bimodal predictor based on an actual branch outcome associated with the branch prediction. (Fig. 8 block 580)

51. As per claim 13, Biles/Yeh teaches the branch prediction architecture of claim 12, wherein the update logic is to update the second global array based on the actual branch outcome if the tag of the branch instruction matched a tag in the second global array. (Fig. 8 block 530)

52. As per claim 14, Biles/Yeh teaches the branch prediction architecture of claim 12, wherein the update logic is to update the first global array based on the actual branch outcome if the tag of the branch instruction matched a tag in the first global array. (Fig. 8 block 530)

53. As per claim 15, Biles/Yeh teaches the branch prediction architecture of claim 12, wherein the update logic is to update the first global array based on the actual branch outcome if the tag of the branch instruction did not match a tag in the second global

array and if the tag of the branch instruction matched a tag in the first global array. (Fig. 8 block 530) *The examiner asserts that if the entry is in the first table, it will be updated regardless of whether it is also found in the second table or not.*

54. Claim 26 is directed toward the same limitations as claim 7, therefore it is rejected under the same grounds as recited above.

Claim 32 is directed toward the same limitations as claim 27, therefore it is rejected under the same grounds as recited above.

2. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biles/Yeh/McFarling in view of Talcott (U.S. Patent No. 6,272,623)

Regarding claim 34, Biles/Yeh discloses the prediction architecture of claim 4.

Biles/Yeh fails to disclose folding the second index to obtain a smaller index for use in indexing into the second global array.

Talcott discloses two branch history tables, including a smaller table with a folded index (col 3 lines 32-60).

In order to save space and limit required resources, Biles/Yeh would have been motivated to allow a folded portion of one table index the other table.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow a first and second global table of Biles/Yeh be indexed using a folded version of the other, similar to the local/global tables shown in Talcott.

55. Claims 1 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biles in view of Alternative Implementations of Two-Level Adaptive Branch Prediction (herein, Yeh-2)

56. As per claims 1 and 33, Biles teaches a branch prediction architecture comprising:

a prediction selector; (Fig. 2b parts 230, 220, 225, 240, 260, 250)

a bimodal predictor (Fig. 2b table 210) coupled to the prediction selector, the bimodal predictor to generate a bimodal prediction for a branch instruction; (Paragraph 59)

and a plurality of global predictors (Fig. 2b tables 205, 207) coupled to the prediction selector, each global predictor to generate a corresponding global prediction for the branch instruction, (paragraphs 58 and 60) the prediction selector to select a branch prediction from the bimodal prediction and the global predictions. (Paragraph 67)

57. Biles but fails to teach wherein each global prediction is to be generated based on a different amount of global branch history information.

58. Yeh-2 teaches two global predictions (page 126 section 2.2) generated based on a different amount of global branch history information (fig. 3).

59. Yeh-2 teaches that utilizing a hybrid predictor of these types can vastly improve performance. See introduction.

60. It would have been obvious to one of ordinary skill in the art at the time of invention to have used Yeh-2's scheme of using differently sized tables in place of Biles' tables

205 and 207 to store branch predictions for the benefit of increasing branch prediction suggest in a larger variety of applications.

61. With further regard to claim 33, Biles/Yeh-2 discloses each prediction being generated an an instruction fetch state of a pipeline.

*Examiner asserts that, unlike the two-level early/late approach shown in Yeh, both of global prediction schemes of Yeh-2 are generated by the fetch state.*

### ***Response to Arguments***

1. Applicant's arguments filed 19 July 2006 have been fully considered but they are not persuasive.

2. Applicant states:

*"The Examiner's conclusion of inherency is based on the assumption that an index must necessarily be the same as a global history information."*

This is false. Examiner stated on page 2 a larger table requires more global history index. These statements are not the equivalent.

Applicant continues:

*"See, for example, FIG 2A of Biles, which clearly shows an index path on 202 being derived from both and [sic] address 20 and history data from a history register 30"*

Applicant appears to have overlooked the last sentence of paragraph [60], "In alternative embodiments, it will be appreciated that the index generation logic may be arranged to generate an index based solely on the history data"

Applicant continues:

*"Thus, increasing the size of an index into a branch prediction table could merely involve increasing the amount of address data being used. In other words, contrary to the Examiner's assertions, such an increase need not, in all cases, require a corresponding increase in the amount of global history being used"*

Examiner never made this assertion. Examiner asserted that an increased size of the branch history table implies an increased size in the index. Applicant chooses to argue the converse—that an increased size of the index doesn't necessarily imply an increased size of the of the branch history table. Examiner fails to recognize how this statement, if true, makes Examiner's rejection improper, even if the alternate embodiment is ignored.

Applicant continues:

*"Simply put, Applicants seasonably traverse the Examiner's assertion of inherency and request evidence to support the conclusion that the claimed approach of using different amounts of global branch history information is a necessary aspect of the cited references."*

Since Applicant appears to be contesting a statement that Examiner never made, it is unclear what documentary support Applicant requires. Examiner will assume that Applicant is contesting the obviousness of an increase in branch history size. As shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range generally would have been obvious improvements.

3. Applicant states:

*"With further regard to claim 6, the Examiner has taken Official Notice "that adding an additional level of storage for global branch predictors is well knkonw in the art." OA p 7. Applicants seasonably traverse this assertion of Official Notice and request documentary evidence supporting it. IN particular, it is not clear that one of ordinary skill in the art would recognize any alleged teachings of "an additiona llevel of storage" as a third global predictor to generate a third global prediction by indexing into a third global array based on a third index, the third index to be associated with a third amount of global branch history length, as claimed."*

Examiner reminds Applicant that a first/second global prediction by indexing a first/second global array based on a first/second index have already been found obvious in claim 3 (a claim on which claim 6 is dependant). Examiner makes the point that it would have been obvious to include an additional level of storage by repeating these same parts. As shown in St. Regis Paper Co. v. Bemis Co. 193 USPQ 8 (7th Cir. 1977), duplicating parts generally would have been an obvious improvement.

4. Applicant states:

*"With specific regard to claim 18, neither Biles nor Yeh teach or suggest each global prediction to be generated based on a different amount of global branch history information as claimed. Applicants reiterate the above traversal of the Examiner's assertion of inherency with regard to the claimed different amounts of global history information and request documentary evidence. The Examiner has also taken Official Notice "that changing the order of multiplexers is well known in the art.") OA p. 9. Applicants seasonably traverse this assertion of Official Notice and request documentary evidence supporting it."*

It is not entirely clear why Applicant does not accept the Official Notice. Examiner asserts that one of ordinary skill in the art would have realized that a common truth table created for either embodiment described by Examiner on page 9 would result on a working and equally usable two-level multiplexer. Examiner has provided Computer Organization and Design by Hennessy and Patterson (herein Hennessy). B9 of Hennessy is attached to show that a multiplexer is created simply using AND, OR, and NOT gates (like any other digital system). B10 of Hennessy is attached to show how logic can be used to create a two-level approach. One of ordinary skill in the art, based on these documents, should be able to determine how a common truth table can logically prove that both techniques discussed are equivalent.

5. Applicant states:

*"In particular, none of the cited references provide for the generation of a plurality of global predictions, wherein each global prediction is to be generated based on a different amount of global branch history information as recited in the claims from which the rejected claims depend"*

Examiner disagrees. On page 5 of the previous office action, Examiner stated, "Yeh's invention discloses branch prediction tables of various sizes (paragraph 10)". Also, not paragraph 8.

6. Applicant states:

*"With further regard to claim 17, the Examiner has taken Official Notice "that storing branch target addresses in a branch prediction table is well known in the art." OA p. 16. Applicant seasonably traverse this assertion of Official Notice and request documentary evidence supporting it"*

A quick search resulted in the following:

Hilgendorf (U.S. Patent No. 5,974,543) col 1 lines 5-12

Dinkjian (U.S. Patent No. 5,822,574) col 2 lines 5-9

Taylor (U.S. Patent No. 5,748,976) col 2 lines 38-42

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sinharoy (U.S. Patent No. 6,976,157) discloses a branch prediction system utilizing both global history and a bimodal predictor.

McFarling et al. (U.S. Patent No. 5,758,142) disclose a system using two different branch prediction methods using different branch histories.

Bonanno et al. (U.S. Publication No. 2004/0225872) discloses a hybrid branch prediction method using both bimodal and global history.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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